AMENDMENTS TO THE CLAIMS

Below is the entire set of pending claims pursuant to 37 C.F.R §1.121(c)(3)(i), with any mark-ups showing the changes made by the present Amendment.

Claims 1-15 (Canceled)

16. (Original) A semiconductor package device, comprising:

a package substrate having a first coefficient of thermal expansion and at least one bonding pad on a surface of the package substrate; and

an integrated circuit chip formed from a semiconductor wafer, the chip comprising:

electrical devices formed therein,

at least one coupling structure for bonding the chip to the at least one bonding pad on the package substrate,

a second coefficient of thermal expansion different than the first coefficient of thermal expansion, and

a final thickness less than a thickness of the semiconductor wafer, wherein the final thickness allows the chip to distort substantially with the package substrate during temperature changes despite the mismatch in their respective coefficients of thermal expansion.

17. (Original) A semiconductor package device according to claim 16, wherein the final thickness is about one-third of the thickness of the semiconductor wafer.

18. (Original) A semiconductor package device according to claim 16, wherein the thickness of the semiconductor wafer is about 29 to 31 mils and the final thickness of the chip is about 3-8 mils.

19. (Original) A semiconductor package device according to claim 16, further comprising a heat spreader coupled to a surface of the chip free of electrical devices.

20. (Original) A semiconductor package device according to claim 16, wherein the at least one coupling structure comprises a metal.

21. (Original) A semiconductor package device according to claim 16, wherein the at least one coupling structure is lead-free.

22. (Original) A semiconductor package device according to claim 16, wherein the at least one coupling structure is a solder ball.

23. (Original) A semiconductor package device according to claim 16, further comprising an inter-metal dielectric layer adjacent to a surface of the chip that is closest to the package substrate, and wherein the at least one coupling structure is located adjacent to the inter-metal dielectric layer.

24. (Original) A semiconductor package device according to claim 16, further comprising a dielectric encapsulant between the chip and the package substrate, the

dielectric encapsulant substantially surrounding the at least one coupling structure and the at least one bonding pad.

25. (Original) A semiconductor package device according to claim 16, wherein the package substrate is selected from the group consisting of glass, ceramic, a silicon-on-insulator, a polymer, silicon, silicon germanium, a single layer printed circuit board having conductive traces formed therein, and a multi-layer printed circuit board having conductive traces formed therein.

26. (Original) A semiconductor package device according to claim 16, wherein the chip comprises at least one coupling structure for metallurgically bonding the chip to the at least one bonding pad on the package substrate.